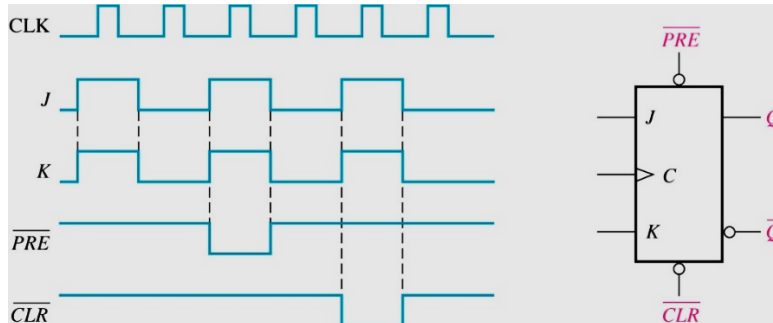


VIRGINIA STATE UNIVERSITY
COMPUTER ENGINEERING
CPEG 207 INTRODUCTION TO DIGITAL SYSTEMS
FINAL EXAM FALL 2020

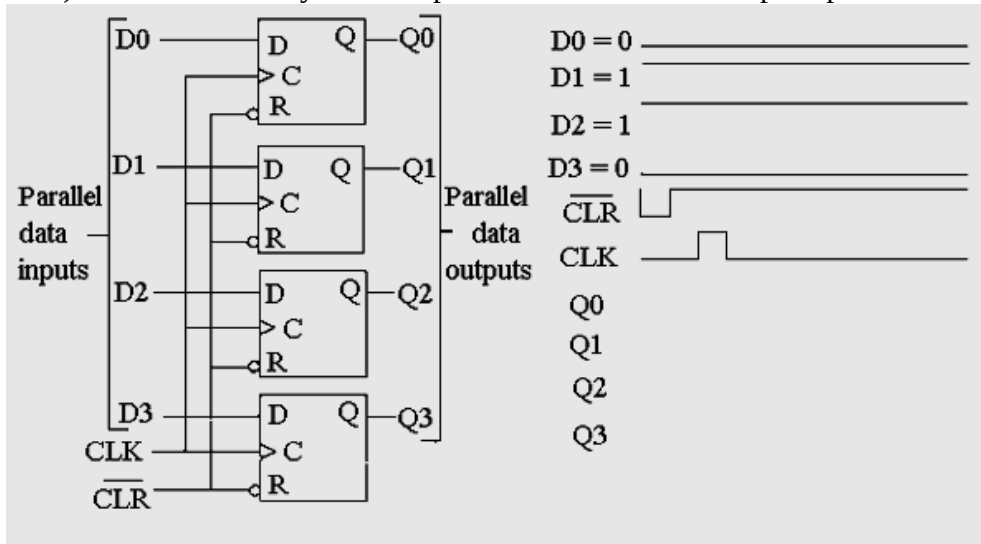
NAME: _____

1. A) For the input waveforms shown below, draw the J-K flip-flop's output Q waveform, assuming that it is initially 0.

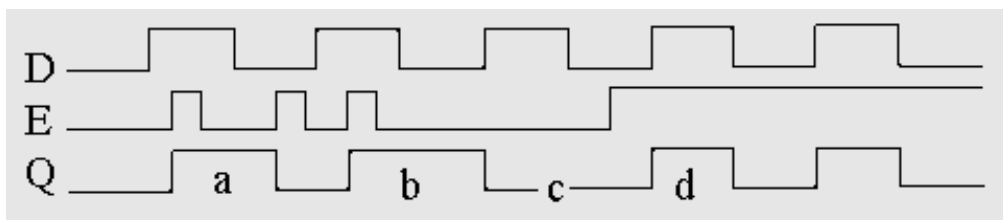


Q

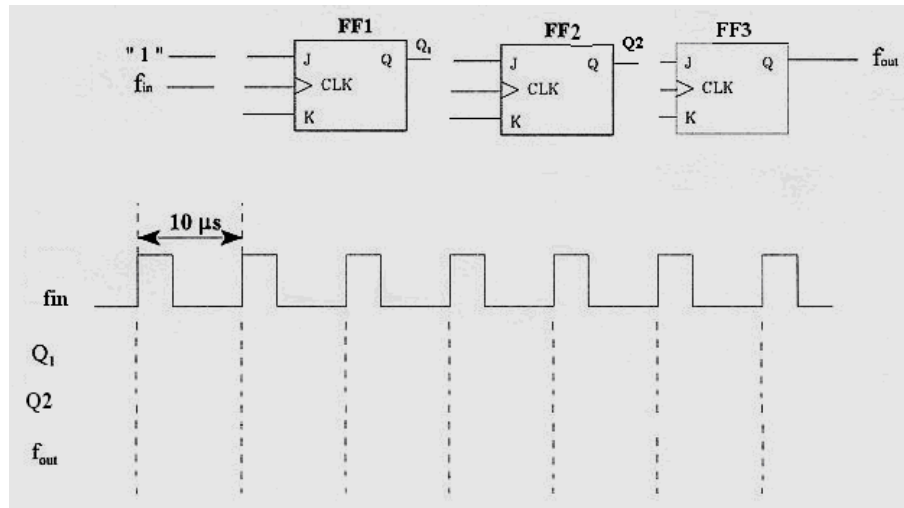
1. B) Draw the initially reset output waveforms for the Flip Flop circuit shown below:



1. C) The waveforms shown in the figure below are applied to a gated D latch, which is initially RESET. Which of the areas identified on the Q waveform is incorrect?

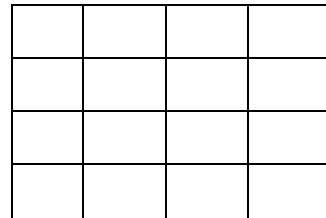
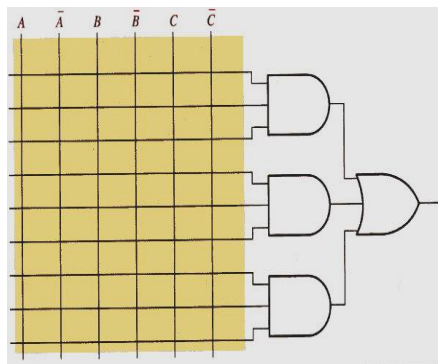


2. A) Connect the three J-K Flip-Flops shown below and draw the timing diagrams showing how the Clock waveform could be used to produce a 12.5 kHz square wave. Note: $f = 1/T$



- 2 B) a) Simplify the following Boolean expression,
 b) connect the PAL array to construct the logic and
 c) write VHDL and Verilog programs to implement the digital circuit.

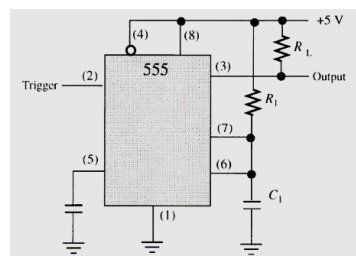
$$X = (\bar{A}\bar{B} + A\bar{B})(CD + \bar{C}\bar{D})$$



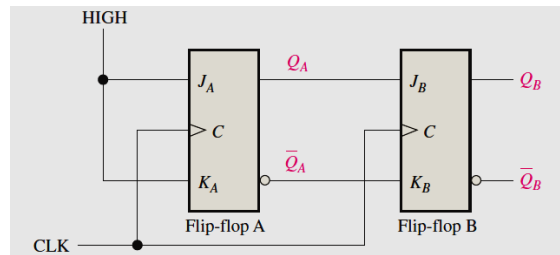
VHDL:
 entity

Verilog:
 module

- 2 C) Determine the standard value of the external resistor R_1 in the 555 timer circuit that will produce a 0.5 s output pulse. Choose the capacitor $C_1 = 1 \mu F$.



2. D) For the circuit , determine the maximum frequency of the clock signal for reliable operation if the set-up time for each flip-flop is 2 ns and the propagation delays (t_{PLH} and t_{PHL}) from clock to output are 5 ns for each flip-flop.



3. A) a) Fill in the following table:

Decimal	Binary	Octal	Hexadecimal	BCD
255				
	1111			

- b) Find the 2's complement of the following binary number:

10111000

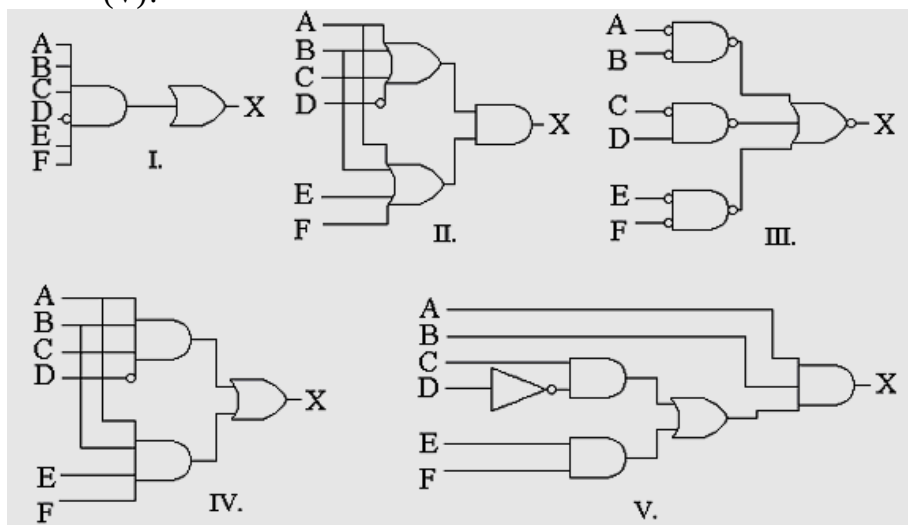
- c) i) Add the following signed numbers and show the equivalent decimal value of the sum:

11011001 + 11100111 =

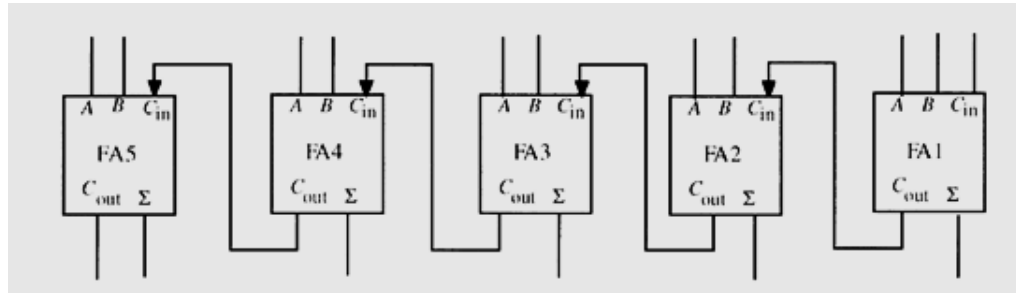
- ii) Add the following hexadecimal numbers:

ABC + DEF =

- 3 B) Which of the circuits in the Figure (I-IV) is the sum-of-products implementation of Figure (V)?

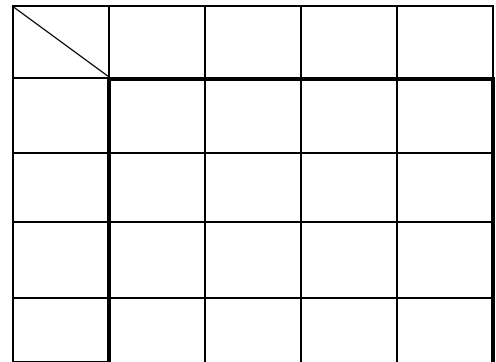


- 3 C) Show the inputs and outputs for the parallel adder shown below, when adding binary 10101 to 00111. Verify your result by longhand addition of the two input numbers and by conversion to decimal numbers.



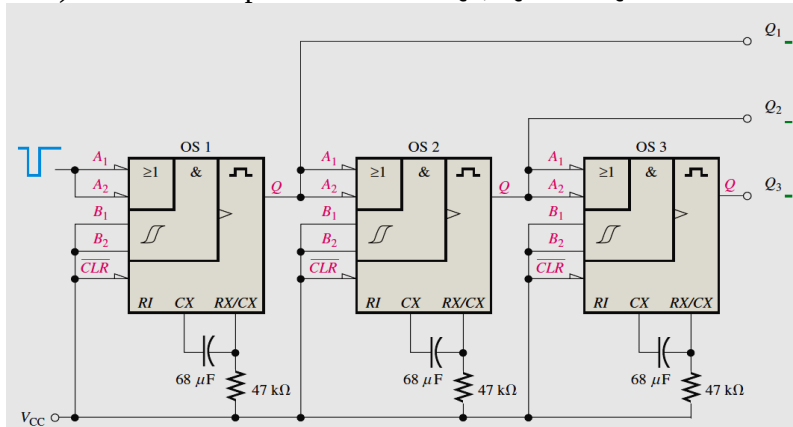
- 4 A) a) Use a Karnaugh Map to obtain a minimum SOP for the Truth Table shown below and

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0



b) draw the digital circuit schematic:

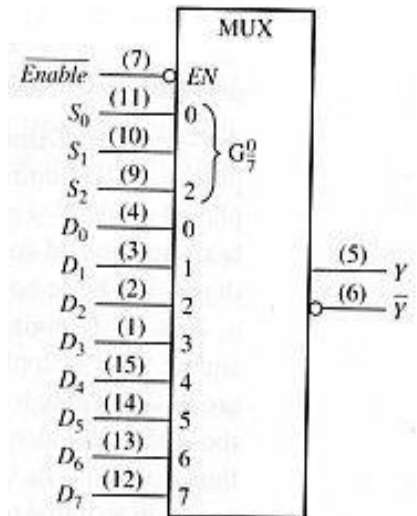
4. B) Draw the output waveforms Q1, Q2 and Q3 of 74122 sequential timing circuit.



4. C) The 74151A is an 8-to-1 Multiplexer. Design a circuit using the 74151A Multiplexer and necessary gate(s) to implement the following logic function. Assume that D is the MSB and A is the LSB.

$$Y = (D+C)(B+A)$$

D	C	B	A	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



5. A) Switches A and B control one of three devices, a motor, a power supply or an alarm in a research facility. Using a 2-to-4 decoder and one appropriate gate, devise a circuit to turn on:

- (a) the motor, referred to as MOTOR, if both switches are closed.
- (b) the power supply, referred to as POWER, if either switch is opened.
- (c) the alarm, referred to as ALARM, if both switches are opened.

Assume these logic levels: Switch closed = 0; Device on = 0
Decoder outputs = active LOW

A	B	MOTOR	POWER	ALARM



2-to-4 decoder

- 5 B) The finance committee of a nine-member legislative committee requires a two-thirds vote to authorize political legislation. The vote is tabulated and put in BCD format. If two-thirds of the committee is in favor of the legislation, an LED is turned on. The LED should be turned on with a LOW logic level. Note also that the BCD bits are D, C, B, A with D the MSB and A the LSB.
- Draw the truth table and Karnaugh map for the problem. Use *don't care* for invalid BCD codes.
- Note: You can either use LED or $\overline{\text{LED}}$ for the K-Map; both will yield the same min SOP.
- Write the minimum SOP for the map.
 - Draw the logic circuit using only 2-input NAND gates. Gate count should not exceed **four**.

D	C	B	A	LED	$\overline{\text{LED}}$

Min SOP:

Logic Circuit:

- 5 C) Using a K-map, find the minimum SOP for the following Truth Table with Don't Care conditions denoted by X. What is the minimum SOP without using Don't Care conditions?

Inputs				Output
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X
